Curriculum Vitae

Name: Ms.P.P.Patil

Address:

42, Vijay Nagar, 0pp. CADA Office, Garkheda, Aurangabad-431001 Dist. –Aurangabad.



E-mail: priti.patil@mit.asia Mobile: 9028384800 Date of Birth: 4th July 1987

AcademicCredentials

Class/	Specialization	Institution	University	Year	%/	Class
Degree					CGPA	
M.E./ M. Tech.	Electronics	Government college of Engineering Aurangabad	Dr.B.A.M. University, Aurangabad	2011	8.34	Distinctio n
B.E./B.Tech.	ETC	Government college of Engineering Jalgaon	North Maharashtra University Jalgaon	2008	70.85 %	Distinctio n

M. Tech. Project: DWT based image compression using VLSI

Key Research Areas: Image Processing

Experience

Sr.	Organization	Post	From To	No. of
No.				Years
1	Maharashtra Institute of	Assistant	1 st August 2012	7 years 6
	Technology, Aurangabad	Professor	to till date	months
2	P.E.S. College of Engineering	Visiting Lecturer	Jan 2010 to April	4
	F.E.S. Conege of Engineering	Visiting Lecturer	2010	Months
3	Bhambhori College of	Lecturer	July 2008 to	10
	Engineering, Jalgaon	Lecturer	April 2009	Months

List of Courses Taught/Teaching at UG level -

- 1. Analog Electronics
- 2. Electronics Measurement
- 3. Basic Electronics
- 4. Electronics Devices and Circuits
- 5. Integrated Circuits and Applications
- 6. HSAD

Membership of Professional Bodies

1. Life Member of ISTE Membership number: LM 107493

Computer/Software Proficiency

- 1. C, C++. MS Windows, MS Office (MS Word, MS Excel, and MS Power Point) & Internet ,MS Office Front page, Photoshop, Flash.
- 2. Hardware & Networking

Seminar/Workshop/Industrial Training/STTP//FDP/CEP/Conference Attended

- 1. Attended a Five days workshop on "System Design Using FPGA(SDF-2013) " at Government college of Engineering Aurangabad from 24th June -28th June 2013.
- Attended a One Day Faculty Development Programme on "Professional English Communication Skills" at Maharashtra Institute of Technology Aurangabad on 17th Jan 2015.
- 3. Attended a One Day workshop on "Research Methodology " at P.E.S. College of Engineering Aurangabad on 20th August 2016.
- 4. Attended One week FDP on "Data Sciences" Funded by MHRD at Maharashtra Institute of Technology, Aurangabad.

Seminar/Workshop/Industrial Training/STTP//FDP/CEP/Conference organized

- Organized Two Days National Level Workshop on "Research Methodology" at Maharashtra Institute of Technology Aurangabad from 13th March 2015 to 14th March 2015.
- Organized Four Days National Level Workshop on "Matlab,Simulink and Low Cost Design using Signal & Image Processing Toolbox"at Maharashtra Institute of Technology Aurangabad during 16th December 2015 to 19th December 2015.
- Organized One Day Hands-on-Training Program on "Need of Electronics in Industry for Electrical and ETC Engineers" For Second Year Student at Maharashtra Institute Of Technology Aurangabad on 20th Feb 2017
- 4. Organized 1st International Conference on "Digital Signal and Image Processing" at Maharashtra Institute of Technology ,Aurangabad on 7th and 8th March 2017.
- 5. Organized IEEE conference AEMC 17 at Maharashtra Institute of Technology, Aurangabad.

NPTEL Certification

Start Date	End Date	Duration	uration Course Name		Performance
		(in Weeks)		(Out of 100)	
March	April	4	TALE	75	

Awards, Achievements and Recognition

Selected as Best Paper Presenter and Got First Prize at Converges'11, A National Level Technical Symposium, organized by R.C.Patel Institute of Technology Shirpur .

Date:28/02/2020

Place: Aurangabad