Curriculum Vitae

Name: Amit Suhas Borole

Address: E503, Kasliwal marvels Tapdia town, Disha nagar, Beside MIT, Beed by Pass Road Aurangabad -431010

E-mail:amit.borole@mit.com Mobile: 8600273686 Date of Birth: 29/08/1990



Academic Credentials

Class/	Specialization	Institution	University	Year	%/CGP	Class
Degree					Α	
GATE	Electrical			2013,	43.67,	
	Engineering			2017,	34.23,	
				2019	38.67	
Ph.D. (Pursuing)	Electrical Engineering	SSBT's COET, Jalgaon	KBC's North Maharashtra University	2018 (admit ted)		
M.Tech.	Electrical Power System	College of Engineering Pune	Pune University	2015	7.75	First class with distinction
B.E.	Electrical Engineering	Government College of Engineering, Jalgaon	KBC's North Maharashtra University	2012	68.00	First class with distinction

M.Tech. Project: Various control schemes for grid connected Voltage Source Inverter Key Research Areas: ---- Power system, Power Electronics

Experience

Sr.	Organization	Post	From To	No. of
No.				Years
1	G.S.Mandal's Maharashtra Institute of Technology Aurangabad (Autonomous)	Assistant Professor (Ad-hoc)	21/12/2021 till date	
2	SSBT'COET, Bambhori, Jalgaon	Assistant Professor (Regular)	23/07/2017 to 20/12/2021	4.5Years
3	Government college of Engineering, Jalgaon (Autonomous)	Assistant Professor (Ad-hoc)	17/05/2016 to 16/04/2017	11 Months
4	G. H. Raisoni, Nagpur (Autonomous)	Assistant Professor (Adhoc)	01/07/2015 to 30/04/2016	11 Months

List of Courses Taught/Teaching at UG level -

- 1) Power System
- 2) Electro Magnetic engineering
- 3) Electrical Circuit Analysis
- 4) Transformer & DC Machines
- 5) Analog and Digital Electronics
- 6) Electrical Drives and Control

Research Projects/Projects Guided ---

- 1) Automatic waste segregation system
- 2) Development of DSTATCOM for power quality improvement
- 3) Development of Grid synchronized Voltage source inverter
- 4) Design and development of solar connected boost converter

Computer/Software Proficiency -- Yes

MS Office, MATLAB, NI_ Multisim, Power world simulator, ETAP, LT SPICE,

Seminar/Workshop/Industrial Training/STTP//FDP/CEP/Conference Attended

- 1) Completed NPTEL course on Design of solar photovoltaic systems
- 2) Attended 5 day STTP on Solar Photovoltaic in NIT Trichy
- 3) Attended one day workshop on Technical paper presentation at IIT Bombay
- 4) Attended 5 day CEP on Design of experiments and data Analysis conducted by GCOEJ and IIT Bombay
- 5) Attended 2 day seminar on research Scholars Conclave at COE, Pune.

List of Research Publications:-

- 1) Published a paper on "Various control schemes for voltage source Inverter in PV grid interfaced system" in IEEE 2015
- 2) Published a paper on "Review on Development of solar power biodegradable waste sorter and composter" in SPRINGER 2020
- 3) Published a paper on "Comparison of PI and PR controller for grid connected voltage source inverter" in international conference ICGTSTHCM 2019
- 4) Published a paper on "Droop controlled technique for Voltage source Inverter in mini grid system by using PI controller" in international journal ICRTES 2017
- 5) Presented a paper on renewable energy systems in National level competition 2014

Declaration

I hereby declare that the information above is true and correct to my knowledge and belief Date: 03/01/2021

Place: Aurangabad.

Signature: