

FACULTY OF ENGINEERING AND TECHNOLOGY
Dr.BAMU Syllabus Structure- 2014-2015
Final year B. Tech (Electronics and Telecommunication Engineering)

Sub Code	SEMESTER-VII	Contact Hrs / Week				Examination Scheme						
		Subject	L	T	P	Total	CT	TH	TW	P	Total	Credits
ETC401	Advanced Embedded System Design	3	1	-	4	20	80	-	-	100	4	3 Hours
ETC402	Microwave and Optical Communication	3	1	-	4	20	80	-	-	100	4	3 Hours
ETC 403	Computer Network and Security	4	-	-	4	20	80	-	-	100	4	3 Hours
ETC404	Wireless and Mobile Communication	4	-	-	4	20	80	-	-	100	4	3 Hours
ETC441-ETC444	Elective-II	4	-	-	4	20	80	-	-	100	4	3 Hours
ETC421	Laboratory-I: Advanced Embedded System Design	-	-	2	2	-	-	50	50	100	1	NA
ETC422	Laboratory-II: Microwave and Optical Communication	-	-	2	2	-	-	50	-	50	1	NA
ETC423	Laboratory-III: Computer Network and Security	-	-	2	2	-	-	50	-	50	1	NA
ETC424	Laboratory-IV: Wireless and Mobile Communication	-	-	2	2	-	-	50	50	100	1	NA
ETC425	Project-II	-	-	6	6	-	-	100	100	200	3	NA
Total of semester-VII		18	02	14	34	100	400	300	200	1000	27	-

Sub Code	SEMESTER-VIII	Contact Hrs /week				Examination Scheme						
		Subject	L	T	P	Total	CT	TH	TW	P	Total	Credits
ETC471	Inplant Training (IPT) *	-	-	-	-	-	-	300	300	600	27	NA
Total of semester-VIII		-	-	-	-	-	-	300	300	600	27	-
Grand Total of VII & VIII		-	-	-	-	100	400	600	500	1600	54	-

L: Lecture hours per week T: Tutorial hours per week P: Practical hours per week CT: Class Test
 TH: University Theory Examination TW: Term Work P: Practical/Oral Examination NA: Not Applicable

Elective-II

ETC441. Analogue VLSI Design

ETC442. Digital Image Processing

ETC443. Electronic Product Design

ETC444. Advanced Industrial Automation

***After every two weeks of Inplant Training (IPT) student shall apprise the progress of training to the internal guide and get the required inputs.**

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No.: ETC401

Teaching Scheme:

Theory: 03 Hrs/ week

Tutorial: 01 Hr/week

Credits:04

Title: Advanced Embedded System Design

Class Test (Marks): 20

Theory Examination (Duration): 03hrs

Theory Examination (Marks): 80

Prerequisites	:	Knowledge of Cross Compiler & Embedded C, Knowledge of Microcontroller based systems & interfacing peripherals.
Course Objectives	:	<ul style="list-style-type: none">• To get students familiar with the typical problems and constraints that arise while designing and developing embedded systems.• To make students capable to design and implement an embedded system, following the model-centric design.• To introduce theoretical and practical solutions to typical problems, that the students are expected to master.
Unit-I	:	Introduction to Embedded System Design: Introduction to Embedded Systems; Architecture, Definitions and constraints; Categories of Embedded Systems; Characteristics; hardware and processor requirements; special purpose processors; design space exploration for constraint satisfaction; co-design approach; Example system design; Formal approach to specification; specification languages; specification refinement and design; design validation; time constraints and performance analysis. [10 Hrs]
Unit-II	:	Introduction to 32 Bit RISC Processor (ARM 7TDMI): Advantages of 32 Bit Processor, Block Diagram and Functions, Pin Diagram, The ARM Core, The ARM Register File, Memory Organization, The AMBA Bus Architecture, The ARM Pipeline, Exceptions and Interrupts, System Memory Map, System Control Blocks Cache & MMU. [10 Hrs]
Unit-III	:	Interfacing Peripherals: On Chip Peripherals like Timers/Counters, Pulse Width Modulator, UART, ADC, DAC, I2C, CAN, RTC, etc. External Peripherals like EEPROM, Stepper Motor, Relay, SSD, LCD, Simple & Matrix keyboard, USB Bus, etc. [10 Hrs]
Unit-IV	:	Real time interfacing: Sensor interfacing like Temperature, Pressure, and Displacement Transducer in Embedded System Environment using High speed ADC & DAC; Wireless sensor networks; Introduction, Applications, Network Topology, Localization, Time Synchronization, Energy efficient, MAC protocols, Energy efficient and robust routing. [10 Hrs]
Unit-V	:	RTOS Overview & Real Time models for ARM: RTOS Task and Task state; Process Synchronization, Message queues, Mail boxes, pipes, Critical section, Semaphores, Classical synchronization problem, Deadlocks. Real time models and languages Event Based; Process Based and Graph based Models, Real Time Languages, RTOS Tasks, RT scheduling, Interrupt processing, Synchronization, Control Blocks, Memory Requirements. [10 Hrs]

Unit-VI	:	Recent trends in Embedded systems: ARM Processor family like ARM9 & ARM11, Processor power, Memory, Operating Systems, Communication interfaces and networking capability, Programming languages, Development tools, Programmable Hardware. [10 Hrs]
Text Books	:	<ol style="list-style-type: none"> 1. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley. 2. Dr. K.V.K.K. Prasad, "Embedded/ Real-Time Systems: Concepts, Design & Programming" Dreamtech Press, New Delhi 3. Steven Furber, "ARM System-on-Chip Architecture", Pearson Education. 4. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997. 5. Sriram Iyer, "Embedded Real time System Programming", Tata McGraw Hill, 2003. 6. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997. 7. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 199
References e- books, e- Journals	:	<ol style="list-style-type: none"> 1. Mr. Gaonkar "Fundamentals of Microcontrollers and Application in Embedded Systems" Penram 2. Stuart Ball "Analog Interfacing to Embedded Microprocessors Real World Design". 3. Breems, "Continuous-Time Sigma Delta Modulations for A/D Conversion". Kluwer, 2002. 4. Bhaskar Krishnamachari, "Networking Wireless Sensors", Cambridge press 2005. 5. ARM Architecture Reference Manual

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

Pattern of Question Paper:

The six units in the course syllabus shall be divided in two equal parts of 3 units each. Question paper shall be set having two sections; Section A and Section B. The questions of Section A shall be set on first part and questions of Section B on second part. Question paper should cover the entire syllabus.

For 80 marks Paper:

1. Set ten questions in all, with five questions in each section.
2. Question no. 1 from section A and Question no. 6 from section B should be made compulsory and should cover the entire course syllabus of the respective section and should be set for ten marks each. The Question no.1 and 6 should be of objective nature.
3. Two questions of 15 marks each from remaining questions from each section A and B should be asked to solve.

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

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Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No.: ETC402

Teaching Scheme:

Theory: 03 Hrs/ week

Tutorial: 01 Hr/week

Credits:04

Title:Microwave and Optical Communication

Class Test (Marks): 20

Theory Examination (Duration): 03Hrs

Theory Examination (Marks): 80

Prerequisites	:	Knowledge of Electromagnetics, Communication , Ray Theory.
Course Objectives	:	<ul style="list-style-type: none">To introduce students to the concepts and principles of the Microwave CommunicationTo introduce students to the concepts and principles of Optical Communication.
Unit-I	:	Introduction to Microwave Wave Guides: Rectangular wave-guide, Wave equation, Modes (TE and TM), Excitation of modes, Power transmission and losses. Microwave cavity resonator, wave guide Tees (E, H, Magic), circulators, isolators, directional coupler, attenuators, phase shifters, ferrite devices, microwave filters, concept of Scattering parameters, S-matrix of above components. [10 Hrs]
Unit-II	:	Microwave Tubes : Microwave Tubes: Two cavity Klystron, reflex klystron, velocity modulation, bunching process, TWT: slow-wave structure, wave modes, gain, and applications , Magnetron oscillator, types. [10 Hrs]
Unit-III	:	Solid-State Microwave Devices: Principle of operation, construction, characteristics, parameters with analysis of Microwave transistor, Varactor Diode, Tunnel, PIN Diode, Gunn Diode, IMPATT, TRAPATT, BARITT. [10 Hrs]
Unit-IV	:	Basics of Fiber Optics: Building blocks of optical fiber communication link, fiber types, ray theory, numerical aperture, optical sources(LED and LASER), optical detectors (PIN APD), fabrication of fiber. [10 Hrs]
Unit-V	:	Signal Degradation in Optical Fiber : Various degradation mechanisms: Attenuation, Dispersion-Intermodal and Intra modal, Pulse broadening in GI fibers, Mode coupling, Coupling losses, Fiber splicing, connectorization, coupling methods and their losses. [10 Hrs]
Unit-VI	:	System Design Considerations and Applications: Analog link, Digital link, point to point link, System Consideration, Link power budget, rise time budget, wavelength division multiplexing, Optical networks: SONET/SDH, Photonic switching and sensor applications, OTDR. [10 Hrs]
Text Books	:	<ol style="list-style-type: none">G. Keiser, "Optical Fiber Communication", McGraw Hill.D. C. Aggarwal, "Fiber Optical Communication".S. Y. Liao, "Microwave Devices & Circuits", Prentice Hall.M. Kulkarni, "Microwave and radar Engineering", Laxmi.
References e- books, e- Journals	:	<ol style="list-style-type: none">John Senior, "Optical Fiber Communication", Prentice Hall.Peter Rizzi. "Microwave Engineering", McGraw Hill.

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

Pattern of Question Paper:

The six units in the course syllabus shall be divided in two equal parts of 3 units each. Question paper shall be set having two sections; Section A and Section B. The questions of Section A shall be set on first part and questions of Section B on second part. Question paper should cover the entire syllabus.

For 80 marks Paper:

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Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering & Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester-VII

Code No.: ETC403

Title: Computer Network and Security

Teaching Scheme:

Class Test: 20

Theory: 4 Hrs / Week

Theory Examination (Duration): 3 Hrs

Credits: 4

Theory Examination (Marks): 80

Prerequisites	:	Digital Communication, Information theory and coding.
Course Objectives	:	<ul style="list-style-type: none">• To interpret the layering concepts in computer networks.• To understand internals of protocols such as HTTP, FTP, SMTP, TCP, UDP, IP• To study different security techniques & its algorithms.
Unit-I	:	Introduction to Computer Networks : Components of Communication Networks, topologies, LAN, MAN, WAN, Broadcast vs Point to Point networks, Overview of network model: ISO - OSI and TCP/IP. Network design issues, service primitives and relationships of services to protocols. [10 Hrs]
Unit-II	:	Physical Layer & Data Link Layer : Communication Media: Twisted pair, coaxial cables, fiber optic cables, Wireless Communication. circuit switching, message switching, packet switching network, framing, error detection and correction, CRC, Elementary protocols – stop and wait, Sliding window, HDLC, PPP. [10 Hrs]
Unit-III	:	Networks, Transport Layer, Application layer : Virtual circuits, and datagram networks, Routing algorithms, Congestion control. Quality of Services Transport layer services and principles. Connectionless v/s connection oriented services like UDP and TCP, FTP, DNS, World wide Web, Voice over IP, Video on demand, M-Bone – Multicast backbone. [10 Hrs]
Unit-IV	:	TCP/IP Protocol Suite : Layered Architecture, Protocol Stack., IP Addressing: Classes, static, dynamic (DHCP), Ipv4 v/s Ipv6, Ping, FTP, SMTP, SNMP, BOOTP, RPC, ICMP, IGMP, ARP, RARP. [10 Hrs]
Unit-V	:	Overview of Network Security: Fundamentals, security services, attacks, overview of cryptography Substitution ciphers, transposition ciphers, Authentication protocols, Authentication based on a shared secret key, Diffie Hellman key exchange, Authentication based on KDC, Authentication using Kerberos. [10 Hrs]
Unit-VI	:	Digital signatures & IP security : Certificates, symmetric key signatures, public key signatures, message digests, MD-5, SHA-1, public key infrastructures, application of IPsec, IPsec protocols, VPN. [10 Hrs]
Text Books	:	<ol style="list-style-type: none">1. A.S.Tanenbaum, "Computer Networks" PHI2. Behrouz A Forouzan, "Data Communications & Networking" TMH
References e- books, e- Journals	:	<ol style="list-style-type: none">1. William Stalling, "Data & Computer Communication" Pearson2. William Stalling, "Cryptography & Network Security" Pearson

Section A: Includes Unit I, II and III; Section B: Includes Unit IV, V and VI.

Pattern of Question Paper:

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For 80 marks Paper:

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(Faculty of Engineering & Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester-VII

Code No.: ETC404

Title: Wireless and Mobile Communication

Teaching Scheme:

Class Test: 20

Theory: 4 Hrs / Week

Theory Examination (Duration): 3 Hrs

Credits:4

Theory Examination (Marks): 80

Prerequisites	:	Modulation Techniques, Time and Frequency Division Multiplexing.
Course Objectives	:	<p>Students will learn</p> <ul style="list-style-type: none"> • Basic concepts of Cellular communication • Building blocks of Mobile communication • Traffic Routing and Grade of Service • Wireless Systems and Standards
Unit-I	:	<p>Introduction: Evolution of mobile radio communication, second generation, third generation, Wireless local loops and LMDS, Wireless Local Area Networks, Bluetooth and Personal Area Networks. [10 Hrs]</p>
Unit-II	:	<p>Cellular Concept: Frequency reuse, channel assignment strategies, Hand-off, Interference and system capacity, Trunking and Grade of service, Improving coverage and capacity in cellular system. [10 Hrs]</p>
Unit-III	:	<p>Mobile radio propagation: Introduction to radio propagation, three basic propagation mechanisms: reflection, diffraction, scattering; practical link budget design using path loss model, indoor and outdoor models, penetration into building, small scale and large scale fading, multipath fading channels types and measurement [10 Hrs]</p>
Unit-IV	:	<p>Equalization, Diversity and channel coding: Fundamentals of equalization , adaptive equalizers, non linear equalizer, Diversity techniques, RAKE receiver, interleaving, Coding, VOCODERS, Linear Predictive Coders, GSM codec, USDC codec [10 Hrs]</p>
Unit-V	:	<p>Wireless Networks: Introduction to wireless networks, Development of Wireless networks, Traffic Routing, wireless data services, comparison between fixed and wireless telephone networks, UMTS [10 Hrs]</p>
Unit-VI	:	<p>Wireless Standards: AMPS and ETACS, IS-54 and IS-136 standard, Global System for Mobile (GSM), CDMA Digital Cellular Standard IS -95, General Packet Radio Service (GPRS), Introduction to LTE Architecture (Long Term Evolution [10 Hrs]</p>
Text Books	:	<ol style="list-style-type: none"> 1. Theodore Rappaport , “Wireless Communications: Principles and Practice” 2nd Edition 2. Lee W.C.Y, “Mobile Cellular Telecommunication Systems” Mc Graw Hill Publication 3. J.G Proakis and M.Salehi , “Communication System Engineering” Prentice Hall 4. John Schiller , “Mobile Communications” 2nd Edition Pearson Education 5. V.K Garg and J.E Wilkes , “Principles and Application of GSM” Pearson Education

References e- books, e- Journals	:	<ol style="list-style-type: none"> 1. David Tse, Pramod Viswanath, “Fundamentals of Wireless Communication”, Cambridge University Press 2005 Wireless Communications and Networks: Recent Advances Author/s: Ali Eksim, Publisher: InTech , 2012 2. Wireless Communications: Signal Processing Perspectives Author/s: H. V. Poor, G. W. Wornell, Publisher: Prentice-Hall, Inc. , 1998 3. Wireless Sensor Networks: Technology and Applications Author/s: Mohammad Matin (ed.), Publisher: InTech , 2012 4. Advanced Wireless LAN Author/s: Song Guo ,Publisher: InTech , 2012
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Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

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Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering & Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester-VII

Code No.: ETC441

Teaching Scheme:

Theory: 4 Hrs / Week

Credits:4

Title: EI-II Analogue VLSI Design

Class Test: 20

Theory Examination (Duration): 3 Hrs

Theory Examination (Marks): 80

Prerequisites	:	It is expected that the student would be familiar with MOS transistor theory, CMOS circuits and knowledge of factors to be considered for CMOS circuit design. Each student is expected to know basic analog integrated circuits design using MOSFET models. Also, each student is expected to be familiar with layout tool and circuit simulator.
Course Objectives	:	<ul style="list-style-type: none">• To make the students able to understand the concepts of analog design and to design various analog systems including data converters- CMOS amplifiers- Comparators and Switched Capacitor Circuits and optimize them with respect to different constraints: size (cost), speed, power dissipation, and reliability.• To acquaint the Students with bottom-up and a top-down design view of Mixed Signal Electronic Systems by the use of modern Computer Aided Design (CAD) tools.
Unit-I	:	Single Stage & Differential Amplifiers: Source Follower, Cascade, Folded Cascade, Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell, Current Sources and Mirrors - Current Sources, Basic Current Mirrors, Cascade Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis. [10 Hrs]
Unit-II	:	Operational Amplifiers: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR. [10 Hrs]
Unit-III	:	Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers, Voltage References - Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References. Feedback - General Consideration Topologies, Effect of Loading. [10 Hrs]
Unit-IV	:	Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques, Noise - Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Figure. Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques. [10 Hrs]

Unit-V	:	PLL & Switched-Capacitor Circuits: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL, Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback. [10 Hrs]
Unit-VI	:	Sampling circuits, ADC & DAC: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures. Input/output characteristics and quantization error of an A/D converter & D/A converter, performance metrics of A/D converter & D/A converter, A/D converter architectures, D/A converter architectures, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions for conversion. [10 Hrs]
Text Books	:	<ol style="list-style-type: none"> 1. D.A.John & K. Martin, "Analog Integrated Circuit Design", Wiley, 1997. 2. Mohamed Ismail, Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill International Editions, 1994.
References e- books, e- Journals	:	<ol style="list-style-type: none"> 1. Razavi, B., "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill (2008). 2. Gregorian, R. and Temes, G.C., " Analog MOS Integrated Circuits for Signal Processing", John Wiley (2004). 3. Allen, P.E. and Holberg, D.R., "CMOS Analog Circuit Design", Oxford University Press (2002) 2nd ed. 4. Johns, D.A. and Martin, K., "Analog Integrated Circuit Design", John Wiley (2008). 5. Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., " Analysis and Design of Analog Integrated Circuits", John Wiley (2001) 5th ed. 6. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2002 VLSI CAD tools.

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

Pattern of Question Paper:

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Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester-VII

Code No.: ETC442

Teaching Scheme:

Theory: 4 Hrs / Week

Credits:4

Title: EI-II Digital Image Processing

Class Test: 20

Theory Examination (Duration): 3 Hrs

Theory Examination (Marks): 80

Prerequisites	:	Nil
Course Objectives	:	This course gives the students the knowledge of fundamentals of Digital Image processing having objectives like <ul style="list-style-type: none">• Students will learn proper image representation, enhancement, filtering, restoration, analysis, reconstruction.• Students will learn advanced digital image processing techniques, including various image transformations, image reconstruction from incomplete information, image segmentation and recognition.
Unit-I	:	Introduction: Digital image representation, fundamental steps in image processing, elements of digital image processing systems, hardware for image processing system, Frame Graber, Characteristics of image digitizer, Image digitizing components, solid state cameras, scanners. Digital image fundamentals: Elements of visual perception, a simple image model sampling and quantization some basic relationship between pixels, Basic transformations, perspective transformation stereo imaging. [10 Hrs]
Unit-II	:	Image Transforms: 2-D Fourier transform, Fast Fourier transform, Other separable transforms, Walsh Transform, Hadamard Transform, Discrete Cosine Transform, wavelet Transform, Haar function. [10 Hrs]
Unit-III	:	Image Enhancement: In Spatial Domain-- Basic Gray Level Transformations , Histogram Processing , Enhancement Using Arithmetic/Logic Operations , Enhancement by point processing, spatial filtering, Enhancement in the frequency domain. [10 Hrs]
Unit-IV	:	Image Restoration: Degradation model, diagonalization of circulant and block-circulant matrices, algebraic approach to restoration, inverse filtering, least mean square (wiener) filter, constrained least squared restoration, invariant restoration, Color image processing. [10 Hrs]
Unit-V	:	Image Compression: Redundancies, image compression models, elements of information theory, error-free compression variable length coding, bit plane coding, lossless predictive coding, lossy compression, predictive coding, transform coding, video compression, image compression standards- JPEG, MPEG. [10 Hrs]
Unit-VI	:	Image Analysis: Segmentation, detection of discontinuities, edge linking and boundary detection, thresholding, region -oriented segmentation, Representation and description: Representation schemes, descriptors, regional descriptors. [10 Hrs]
Text Books	:	1. R. C. Gonzalez, R. E. Woods, "Digital Image Processing", Pearson Education. 2 nd edition, 2002

		2. Anil K. Jain, “Fundamentals of Digital Image Processing” , Prentice Hall of India. 3. Pratt W.K. “Digital Image Processing”, Third Edition, John Wiley & Sons, 2001
References e- books, e- Journals	:	1. B. Chanda & D. Dutta Majumder, “ Digital Image Processing and Analysis”, 2001 2. A. Bovik, “Handbook of Image & Video Processing”, Academic Press, 2000

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

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(Faculty of Engineering & Technology)

Syllabus of Final Year B. Tech. (**Electronics and Telecommunication Engineering**) Semester-VII**Code No.:** ETC443**Teaching Scheme:****Theory:** 4 Hrs / Week**Credits:**4**Title:**EL-II Electronic Product Design**Class Test:** 20**Theory Examination (Duration):** 3 Hrs**Theory Examination (Marks):** 80

Prerequisites	:	Nil
Course Objectives	:	<ul style="list-style-type: none">▪ To make the student aware of major issues and techniques of electronic product design.
Unit-I	:	PCB Fabrication Technology: Soldering techniques, Solderability testing, Study of packages for discrete devices & ICs, IC reliability issues, Parasitic elements, Calculations of parasitic elements in high speed PCB, High speed PCB design, Mounting in presence of vibration, SMD assemblies Board layout check list, Tests for multilayer PCB Cables. [10 Hrs]
Unit-II	:	Product Design & Development: Introduction, Stages in product design & documentation, Electronic Products Classification, Bath tub curve, Redundancy, Failsafe system, Ergonomic & aesthetic design considerations, Power supply design, Noise in electronic circuit, & Measurement of noise. [12 Hrs]
Unit-III	:	Hardware design and testing methods: Design issues related to analog, digital and mixed circuits, Testing of signal conditioning, Data acquisition, MOS, Processor System Circuits, Use & limitations of different types of analysis, Monte Carlo analysis. [10 Hrs]
Unit-IV	:	Software design and testing methods: Different approaches to development of application software for Electronic Product , Goals & Phases of software design, Methods of program flow representation, Testing & debugging of program, Software design, Finite state machine, Comparison of machine level and high level language, Hardware Test Programs. [08 Hrs]
Unit-V	:	Product testing and EMI/EMC: Introduction, EMI/EMC interference & remedies, EMI/EMC regulations, noise coupling, EMI in electronic systems, types, Conducted emission test, Radiated emission test, , Cabling & Wiring of Electronic Systems, Shielding & grounding, Electrostatic Discharge, Protection Against Electrostatic Discharges, Electromagnetic compatibility & testing. [10 Hrs]
Unit-VI	:	Packaging & Enclosures of Electronic System: Effect of environmental factors on electronic system, Materials used for electronic systems, Types of packaging, Packaging's influence and its factors, Cooling in/of Electronic System - Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection. [10 Hrs]
Text Books	:	<ol style="list-style-type: none">1. R.G.Kaduskar, V.B.Baru, "Electronic Product Design", Wiley India2. Bernhard E. Bürdek, "History,Theory and Practice of Product Design", Springer Science, 20053. Paul Horowitz, "Art of Electronics", Cambridge University Press

		<ol style="list-style-type: none"> 4. Charles Kitchin and Lew Counts “A Designer’s Guide to Instrumentation Amplifiers”; Seminar Materials 5. Howard Johnson, Martin Graham, “High-speed Digital design- A Handbook of Black Magic”, Prentice Hall Publication 6. W Bosshar “Printed Circuit Boards - Design & Technology”, 1st edition, Tata McGraw Hill 7. Eamon Nash “Errors and Error Budget Analysis in Instrumentation Amplifier Applications”, Application note AN-539 8. Tim Williams, “EMC for Product Designers”, Elsevier, Fourth edition 2007
References e- books, e- Journals	:	<ol style="list-style-type: none"> 1. http://www.analog.com 2. Pressman , “Software Engineering - A Practitioner's Approach”

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

Pattern of Question Paper:

The six units in the course syllabus shall be divided in two equal parts of 3 units each. Question paper shall be set having two sections; Section A and Section B. The questions of Section A shall be set on first part and questions of Section B on second part. Question paper should cover the entire syllabus.

For 80 marks Paper:

1. Set ten questions in all, with five questions in each section.
2. Question no. 1 from section A and Question no. 6 from section B should be made compulsory and should cover the entire course syllabus of the respective section and should be set for ten marks each. The Question no.1 and 6 should be of objective nature.
3. Two questions of 15 marks each from remaining questions from each section A and B should be asked to solve.

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering & Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester-VII

Code No.: ETC444

Title: EI-II Advanced Industrial Automation

Teaching Scheme:

Class Test: 20

Theory: 4 Hrs / Week

Theory Examination (Duration): 3 Hrs

Credits:4

Theory Examination (Marks): 80

Prerequisites		Nil
Course Objectives	:	The trend in the Industry for automation is changing one and student will able to develop the skill set for latest development of automation.
Unit-I	:	Basic of Automation: Introduction of sensors , actuators, control loop, concept of process variables, set point, controlled variable, manipulated variable, load variable. Representation of process loop components using standard symbols (basic with reference to control loop), and Examples of process loops like temperature, flow, level, pressure etc. Hierarchical levels of automation, introduction to plant automation. [10 Hrs]
Unit-II	:	Transmitters and Converters: Need of transmitter (concept of field area & control room area), Need for standardization of signals, current, voltage and pneumatic signal standards, concept of live & dead zero, DPT, span & zero adjustment, Two wire transmitter, SMART transmitter: Comparison with conventional transmitter, Block schematic converters, Difference between converter & transmitter, Pneumatic to current converter, current to pneumatic converter. Switches: Temperature, pressure, Level switch, Proximity switch, Reed switch, Contactors. [10 Hrs]
Unit-III		Actuators: Types of control valves, Control valve terminology Range ability, turndown, valve capacity, Air to open, Air to close, valve gain etc. Control valve characteristics: Inherent & installed control valve accessories. Positioners: Application/Need, Types, Effect on performance of control valves. Volume boosters, Pressure boosters, Reversing relay, Solenoid valves, Airlock, position indicating switches, Electro pneumatic converter, hand wheel. Brief of stepper motor, servo motor, Motor control circuits, AC drives, DC drives, VF drives, PWM Techniques. [10 Hrs]
Unit-IV	:	Programmable Logic Controller (PLC) Continuous versus Discrete Process Control, ladder diagram using standard symbols, architecture of PLC, types of Input & Output modules (AI, DI, AO, DO), types of Timer, Counter, interfacing pneumatic & Hydraulic systems, fixed & modular PLC (Rack, Slot, Grouping), Specification, manufacturers, PLC ladder diagram and instructions, PLC programming for process applications. Supervisory control system and data acquisition (SCADA): Introduction to SCADA, SCADA architecture, creation of data base, interfacing with PLC. [10 Hrs]
Unit-V	:	Industry Standard Protocols HART protocol introduction, frame structure, programming, implementation examples, benefits, advantages and limitations. Introduction to Foundation Fieldbus H which includes structure, programming,

		FDS configuration, implementation examples, benefits, advantages and limitations, comparison with other field bus standards like Devicenet, Profibus, Profinet, Controlnet, CAN, industrial Ethernet. [10 Hrs]
Unit-VI	:	Distributed Control Systems Basics: DCS introduction, functions, advantages and limitations, DCS as an automation tool to support Enterprise Resources Planning, DCS Architecture of different makes, Latest trends and developments. DCS detail engineering, specifications, configuration and programming, functions including database management, reporting, alarm management, communication, third party interface, control and display. [10 Hrs]
Text Books	:	<ol style="list-style-type: none"> 1. Curtis D. Johnson, “Process Control Instrumentation Technology” ,PHI 7th edition 2. Garry Denning, “Introduction to Programmable Logic Controller”, Thomson Learning.
References e- books, e- Journals	:	<ol style="list-style-type: none"> 1. Emerson Process Management , “Control Valve Handbook” 4th edition. 2. Andrew and Williams, “Applied Instrumentation in Process Industry”, Gulf Publication. 3. B.G.Liptak, “Instrumentation Engineers Handbook: Process Control” ,Chilton book company.

Section A: Includes Unit I, II and III; **Section B:** Includes Unit IV, V and VI.

Pattern of Question Paper:

Pattern of Question Paper:

The six units in the course syllabus shall be divided in two equal parts of 3 units each. Question paper shall be set having two sections; Section A and Section B. The questions of Section A shall be set on first part and questions of Section B on second part. Question paper should cover the entire syllabus.

For 80 marks Paper:

1. Set ten questions in all, with five questions in each section.
2. Question no. 1 from section A and Question no. 6 from section B should be made compulsory and should cover the entire course syllabus of the respective section and should be set for ten marks each. The Question no.1 and 6 should be of objective nature.
3. Two questions of 15 marks each from remaining questions from each section A and B should be asked to solve.

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No: ETC421

Title: Laboratory I: Advanced Embedded System Design

Teaching Scheme:

Term Work (Marks): 50

Practicals: 02 Hrs/week

Credits: 01

Practical Examination (Marks): 50

Course Objectives	:	To acquaint the learners with modern tools like Programmers, Debuggers, Cross compilers and current IDE i.e. integrated development environment tools so that learner can design, implement and test an embedded system with the skills of Embedded C.
List of Practicals	:	Experiments: <ol style="list-style-type: none">1. LED Patterns: Generate any four random patterns on LED Matrix.2. Square wave Generation: Create square wave at any GPIO of ARM using timer function.3. ARM to PC Communication via UART Transmit a message via UART of ARM and display it on Terminal of PC.4. Decimal Counter and Multiplexing the Output: Implement a decimal counter, which counts from 0 to 99 on SSD.5. Keyboard interfacing Sense key and display the appropriate code on SSD. Step Motor Controller6. Implementing I2C Communication Protocols: Interface EEPROM using I2C Communication protocols. .7. LCD Interface: Interface LCD with ARM using only 4 pins8. IR Remote Control Receiver: Implement IR remote control receiver using ARM9. Implementation of simple calculator using ARM 7TDMI: Implement a simple calculator using ARM 7TDMI with keyboard and LCD display interface.10. A Temperature Monitoring and Acquisition System with LCD Output and memory interface.
List of Reference Books	:	<ol style="list-style-type: none">1. Steven Furber, "ARM System-on-Chip Architecture", Pearson Education2.2. Dr. K.V.K.K.Prasad "Embedded/ Real-Time Systems: Concepts, Design Programming" Dreamtech Press, New Delhi3. ARM Architecture Reference Manual Stuart Ball "Analogue Interfacing to Embedded Microprocessors Real World Design".

Term Work assessment shall be done on the basis of

- Performing the experiments in the laboratory and
- Continuous assessment

Practical Examination shall be conducted on the syllabus and term work mentioned above.

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No: ETC422

**Title: Laboratory II: Microwave and Optical
Communication**

Teaching Scheme:

Term Work (Marks): 50

Practicals: 02 Hrs/week

Credits: 01

Course Objectives	:	<ul style="list-style-type: none">In this laboratory students will learn to measure and analyze characteristics of microwave devices and optical components.
List of Practicals	:	Experiments: <ol style="list-style-type: none">To study Microwave components.Measurement of attenuation.Measurement of coupling factor and directivity of directional coupler.Measurement of frequency of microwave source and demonstrate relationship among frequency, free space wavelength and guided wavelength.To plot VI characteristics of Gunn Oscillator.Measurement of insertion loss and isolation loss of three port circulator.To plot electrical characteristics of source and DetectorNumerical Aperture measurement of fiberAttenuation Measurement of fiberEye pattern MeasurementBER measurement.Losses measurement in optical fiber.
List of Reference Books	:	<ol style="list-style-type: none">Gerd Keiser, "Optical fiber Communication", MGH Publication.Robert Collin, "Foundation for Microwave Engineering" Willy Student Edition.

Term Work assessment shall be done on the basis of

- Performing the experiments in the laboratory and
- Continuous assessment

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No: ETC423

Title: Laboratory III: Computer Network and Security

Teaching Scheme:

Term Work (Marks): 50

Practicals: 02 Hrs/week

Credits: 01

Course Objectives	:	<ul style="list-style-type: none">In this laboratory students will learn various aspects of computer network and security issues using simulation tools
List of Practicals	:	Experiments: <ol style="list-style-type: none">Study of LAN transmission medias, topologies, interconnection devices .Design and analysis of network and backbone Using simulation tools.Simulation of error detection and correction code.Network Analysis based decision system for Admission control, congestion control, capacity planning using simulation tools.Design and analysis of routing algorithm for network measurements using network simulation tools.Network planning and implementation: Bandwidth issue, Security Issues using network simulation tool.Write a program for encryption & decryption using substitution ciphers.Study of web page design using HTML.Study of video on demand.Study of Digital Signatures.Study of FTP & SMTP,SNMP protocols.Study of Address Resolution Protocol.
List of Reference Books	:	<ol style="list-style-type: none">A.S.Tanenbaum , “Computer Networks” PHIBehrouz A Forouzan, “Data Communications & Networking” TMHWilliam Stalling , “Data & Computer Communication” PearsonWilliam Stalling , “Cryptography & Network Security” Pearson

Term Work assessment shall be done on the basis of

- Performing the experiments in the laboratory and
- Continuous assessment

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad (Faculty of Engineering and Technology) Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII		
Code No: ETC424		Title: Laboratory IV: Wireless and Mobile Communication
Teaching Scheme:		Term Work (Marks): 50
Practicals: 02 Hrs/week		Practical Examination (Marks): 50
Credits: 01		
Course Objectives	:	<ul style="list-style-type: none"> • To study the working of GSM transreceiver • To study the modulation used in GSM and CDMA. • To Study the AT commands
List of Practicals	:	Experiments: <ol style="list-style-type: none"> 1. To understand the basic circuit of mobile phone(transmitter, receiver & base band control section). 2. To study working of a SIM card in GSM handset, SIM card detection. 3. To study and analyze the Vibrator in GSM handset, at alarm time on, charging Phenomenon in GSM handset. 4. To study the row /column configuration of Matrix keypad. 5. Measure and plot GMSK signal such as transmitter and receiver signal 6. To study and analyze the LCD module used in display section of mobile handset. 7. To study AT commands using GSM trainer module. 8. To study CDMA transmitter and receiver. 9. To study constellation diagram of CDMA transmitter and receiver 10. To study General Packet Radio Service.
List of Reference Books	:	<ol style="list-style-type: none"> 1. Theodore Rappaport , “Wireless Communications: Principles and Practice” 2nd Edition 2. Lee W.C.Y, “Mobile Cellular Telecommunication Systems” Mc Graw Hill Publication 3. J.G Proakis and M.Salehi , “Communication System Engineering” Prentice Hall 4. John Schiller , “Mobile Communications” 2nd Edition Pearson Education 5. V.K Garg and J.E Wilkes , “Principles and Application of GSM” Pearson Education

Term Work assessment shall be done on the basis of

- Performing the experiments in the laboratory and
- Continuous assessment

Practical Examination shall be conducted on the syllabus and term work mentioned above.

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VII

Code No: ETC425

Title: Project-II

Teaching Scheme:

Term Work (Marks): 100

Practicals: 06 Hrs/week

Credits: 03

Practical Examination (Marks): 100

Course Objectives	: <ul style="list-style-type: none">• The practical implementation of theoretical knowledge gained during the study to till date is important for engineering education. The student should be able implement their ideas/real time industrial problem / current application of their engineering branch which they have studied in curriculum.• To motivate students for creativity.• To create awareness regarding latest technology• To have common platform for interaction about emerging technology.• To inculcate qualities of team work.• To explore related information using books, research papers, journals & websites.• To improve presentation and communication skills.
List of Practicals	: <p>Guidelines For Students And Faculty:</p> <ol style="list-style-type: none">1. Students shall complete the Project-II in continuation of the work planned in third year under the course Project-I2. Each student/group is required to-<ol style="list-style-type: none">a. Submit a report with latest status of the project work.b. Give a 10 minutes presentation through OHP, PC, and Slide projector followed by a 10 minute discussion in the second week of their academic semester.c. Submit a report on the project topic with a list of required hardware, software or other equipment for executing the project in the third week of their academic semester.d. Start working on the project and submit initial development and CPM/PERT planning drawing in the fourth week of their academic semester.e. Preparation of PCB layout, wiring diagram, purchase of components, software demo, flowchart, algorithm, program/code, assembling, testing, etc. should be submitted by student/s within next five/Six weeks and minimum one page report should be there for each major activity.f. Overall assembling, wiring, code writing, testing, commissioning along with performance analysis, should be completed within next two weeks.g. In the last week, student/group will submit final project report to the guide.3. Every assigned faculty/s should maintain record of progress of each student or group. <p>The format and other guidelines for the purpose of the Project Submission in hard bound copies should be as follows,</p>

	<p>REPORT STRUCTURE Index/Contents/Intent List of Figures List of Tables List of Symbols / Abbreviations 1. Introduction 2. Literature survey 3. System development 4. Performance analysis 5. Conclusions References Appendices Acknowledgement</p>
	<p>1. INTRODUCTION 1.1 Introduction 1.2 Necessity 1.3 Objectives 1.4 Theme 1.5 Organization 2. LITERATURE SURVEY Literature Survey Related information available in standard Books, Journals, Transactions, Internet Websites <i>etc.</i> till date (More emphasis on last three to five years) 3. SYSTEM DEVELOPMENT Model Development</p> <ul style="list-style-type: none"> • Mechanical / Fabricated • Analytical • Computational • Experimental • Mathematical • Software <p>(out of above methods at least one method is to be used for the model development) Some mathematical treatment or related information is required to be embodied 4. PERFORMANCE ANALYSIS</p> <ul style="list-style-type: none"> • Analysis of system developed either by at least two methods depending upon depth of standard • These methods normally used are Analytical /Computational/Statistical/Experimental/ or Mathematical • Results at various stages may be compared with various inputs • Output at various stages with same waveforms or signals or related information/parameters • Comparison of above results by at least two methods and justification for the differences or error in with theory or earlier published results <p>5. CONCLUSIONS 5.1 Conclusions 5.2 Future Scope 5.3 Applications</p>

	<p>Contributions (if any) The innovative work/invention/new ideas generated from the analysis of the work which can be taken from the conclusions</p> <p>REFERENCES</p> <ul style="list-style-type: none"> • Author, “Title”, Name of Journal/Transactions/ Book, Edition/Volume, Publisher, Year of Publication, page to page (pp.____). <p>These references must be reflected in text at appropriate places in square bracket In case of web pages complete web page address with assessing date has to be enlisted List of references should be as per use in the text of the report</p> <p>APPENDICES Related data or specifications or referred charts, details computer code/program, etc.</p> <p>ACKNOWLEDGEMENTS Expression of gratitude and thankfulness for helping in completion of the said task with name & signed by the candidate</p>
	<ul style="list-style-type: none"> • General Guidelines <p>Text should be printed on front and correct side of the watermark on quality bond paper Paper size- A4, 75 to 85 gsm paper Left Margin-1.5” Right Margin-3/4” Top Margin-1” Bottom Margin-1”</p> <ul style="list-style-type: none"> • Pagination <p>First page of every chapter need not be printed but counted, second page onwards page number to printed at bottom center place. All Greek words must be italic</p> <p>Report Heading -ALL CAPITAL—16 Font Chapter heading -ALL CAPITAL—14 Font Subchapter –Title Case-12 Font Sub-Subchapter –First Alphabet Capital case-12 Font Page numbers for Index/Contents/Intent should be in roman All text should be in times new roman Cover page should have complete symbol of institute Suitable flap (bookmark) with name of the candidate, Department and Institute name and symbol can be used with nylon strip.</p>
	<p>For more information and sample of hard copy please contact the respective Head of the Department.</p>

Dr. Babasaheb Ambedkar Marathwada University, Aurangabad

(Faculty of Engineering and Technology)

Syllabus of Final Year B. Tech. (Electronics and Telecommunication Engineering) Semester VIII

Code No: ETC471

Title: Inplant Training

Teaching Scheme:

Term Work (Marks): 300

Practicals: 06 Hrs/week

Credits: 27

Practical Examination (Marks): 300

Rationale	(a)	The techniques and processes of production of goods and services do not demand only technical skills, but also a cluster or conglomerate of skills. A significant part of which is related to the total humanistic growth of the man. Such conglomerate skills technical and humanistic cannot obviously be acquired through pure academic learning of concepts in formalized and institutional courses and in isolation of the actual work situation. It, therefore, naturally follows that no technical education will be complete till it has two components, one learning of concepts vis-a vis acquiring conceptual skill and other application of the concepts in real work situation vis-a vis acquiring manipulative or practicing skills. Technical education needs to have a complement of learning of the techniques of applying the concepts within the industry and business.
Objectives	(b)	1) The students of B.Tech course shall get an opportunity to work on live problems of the industry. 2) He/She shall apply his learning concepts in the real work situation. 3) He/She shall get an exposure to the industrial environment and thereby enable himself/herself to appreciate the other related aspects of industry vis, human, economic, commercial and regulatory. 4) He/She shall identify career paths taking into account their individual strengths and aptitude. 5) He/She shall contribute for the achievement of economic goals and aspirations of the industry and our country as a whole.
	(c)	The curriculum for B.Tech students of Final Year Course of Part-II shall consist of; 1) Inplant training for a period of one full term, and the period of the term shall be as prescribed by the university from time to time 2) A project on live problems of the industry shall be undertaken by the student/group of students undergoing training in the same establishment. 3) The term work shall consist of the inplant training record-daily diary, work diary, progress report, a record containing the literature survey in the field of appropriate branch of Engineering, a preliminary report related to project work etc. 4) Seminars will be arranged after successful completion of period specified in the scheme of semester VIII of B.Tech. The date and times will be decided according to the convenience of guide and student.
	(d)	Memorandum of understanding: Maharashtra Institute of Technology, Aurangabad will enter into an agreement with the industry through 'Memorandum of Understanding' for creating facilities of inplant training in the appropriate branch of Engineering according to the Course Curriculum and keep this agreement for a period of 10 years to foster a

		healthy industry- institute interaction for mutual benefits of both.
		<p>Admission to inplant training: No student will be deputed for inplant training unless he produces testimonial of having kept one term for the subject under B Tech Semester –VIII of final year course satisfactorily in Maharashtra Institute of Technology after passing the TY B Tech Examination (in the appropriate branch).</p>
		<p>Period of inplant training: The period of Inplant training will be the period of one term for the subject under B Tech course semester-VIII, which will be notified by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad.</p>
		<p>Contract of Inplant Training :</p> <ul style="list-style-type: none"> • The student of Maharashtra Institute of Technology shall enter into a contract of inplant training with the employing industry. • The inplant training shall be deemed to have commenced on the date, on which the contract of inplant training has been entered into. • Every contract of inplant training will contain the Terms and Conditions to be agreed by both the parties. • Every contract of inplant training shall be registered with the Maharashtra Institute of Technology within 15 days from entering into the contract.
		<p>Violation of contract: Where an employer, with whom a contract for inplant training has been entered into, is for any reason, unable to fulfill his obligation under the contract, the contract end with the consent of Maharashtra Institute of Technology. It is agreed between the employer, the student and any other employer that the student shall be engaged as an “inplant trainee” under the other employer till the expiry period of the inplant training. The agreement on registration with Maharashtra Institute of Technology shall be deemed to be the contract of inplant training between the student and other employer, and from the date of such registration, the contract of inplant training with the first employer shall terminate and no obligation under that contract shall be enforceable at the instance of any party to contract against the other party thereto.</p>
		<p>Termination of Contract: The contract of inplant training shall terminate on the expiry of the period of inplant training. Either party to the contract of inplant training make an application to Maharashtra Institute of Technology, Aurangabad for the termination of the contract. After considering the content of the application, and objection, Maharashtra Institute of Technology by order in writing, will terminate the contract, if it is satisfied that the parties to the contract have/has failed to carry out the Terms and Conditions of the contract. Provided that where a contract is terminated-</p> <ul style="list-style-type: none"> • For the failure on the part of the Employer, Maharashtra Institute of Technology will depute students to another Employer for providing facilities of inplant training to the remaining period of training. • For the failure on the part of the student, the student will not be allowed to continue his/her inplant training in that term. The student shall be deputed

		for inplant training in the next coming term.
		<p>Expectation from the Employer / Industry / Establishment: The following expectations are derived for effective inplant training.</p> <ol style="list-style-type: none"> 1. To provide legitimate facilities for the training and learning of all the processes. 2. To guide the student for understanding a project of immense importance to industry and to help him/her for his/her career advancement.
		<p>Obligation of Students:</p> <ul style="list-style-type: none"> • To learn his/her subject field in Engineering or Technology conscientiously and diligently at his place of training. • To carry out all orders of his Employer and the Superior in the establishment. • To abide by the Rules and Regulations of the Industry/Establishment in all matters of conduct and discipline. • To carry out the obligation under the contract of inplant training. • The student shall maintain a report of his work during the period of his inplant training in a proforma (form no: 2) made available in Annexure. • Except in case of extreme urgency, the B.Tech student shall submit an application for all other leaves except the medical leave to the Manager/Gen. Manager (Personnel) of the concerned industry, where he is undergoing an inplant training and obtain sanction before the leave is taken. In case of Medical Leave, he shall submit an application to Maharashtra Institute of Technology, Aurangabad. The shortage in attendance will be subjected to extending the period of inplant training in which case, the student may not be allowed to appear for the test, project seminar and assessment of term work etc. which will be held immediately after successful completion of the inplant training.
		<p>Maintenance of Record: Every student of B.Tech course shall maintain a daily record of the work done by him/her relating to the inplant training in the proforma (Annexure).</p>
		<p>Industry Sponsored Student Projects: The scheme envisages working out suitable programme for B.Tech students. They are required to complete their inplant training in a given period. During this period, they shall be familiar with the understanding of the shop process and activities. The students can be asked to solve the mini-shop problem, which will make them think and try out short experiments as an improvement in the process, tools and equipment. The student here is not expected to acquire the skills in operating machines values. He should appreciate the application of theory learnt. The students in a group alone can undertake a project of immense importance for the benefit of the industry and also useful for the students for their advancement of career. Industry staff and Maharashtra Institute of Technology faculty can plan in advance to effectively complete the practical training with the project for preliminary studies on the floor. The projects should aim mainly-</p> <ul style="list-style-type: none"> • Cost reduction • Reducing cycle time

	<ul style="list-style-type: none"> • Enhancing productivity • Energy conservation measures • Process Improvement technique • Inventory control • Quality control Technique • Improvement in Material handling system • Bottlenecks in material flow system and so on. • Live problems in the industry. • Application development using electronics related knowledge. • EMI/EMC related issues.
	<p>What will form a good project? Through the project, it is hoped to provide the students an exciting experience in solving line problems under practical constraints. Hence it is desired that the project should be a well-defined problem, which can be completed and implemented within the project period. It may be a problem, evolving analysis, design, fabrication and / or testing.</p>
	<p>Time Schedule for the Project: The following time schedule should be planned by each student or groups of students, who undertake the project.</p> <ul style="list-style-type: none"> • Proposal to be received before specified date. • Project acceptance before. • Commencement of the project. • Completion of the project.
	<p>Commitment on the part of the Institute:</p> <ul style="list-style-type: none"> • Providing a faculty member to supervise the project. • Providing the Institute facilities to complete the project. • Coordinator from industry will be invited to participate in the stage wise assessment of the students performance.
	<p>Assistance for completion of the Project: All the projects undertaken by the students are time bound. Although, every attempt results may not be achieved within the period available for the student. In such cases, the services of the associated faculty members can be sought for the completion of the same on mutually agreed terms.</p>
	<p>Monitoring of Inplant Training: The B.Tech students are expected to follow all the rules and discipline of the industry. However, because of other academic requirements and the nature of the project, the student may have to work in other places outside the industry. The faculty and Industry supervisor will work out a suitable arrangement to review the progress of the work from time to time. Maharashtra Institute of Technology, Aurangabad will monitor the progress of inplant training in association with industry authority.</p>
	<p>Conduct and Discipline: In all matters of the conduct and discipline, B.Tech student shall be governed by the rules and regulations (applicable to employees of the corresponding category)</p>

		in the Establishment, where he/she is undergoing a training.
		<p>B.Tech Students are Trainees and not Workers:</p> <ul style="list-style-type: none"> • Every B.Tech student undergoing an inplant training in the respective branch of Engineering & Technology in any Establishment shall be treated as a trainee and not a worker and- • The provision of any law with respect to labour will not apply to such a trainee.
		<p>Settlement of Disputes:</p> <p>Any disagreement or dispute between an industry and a B.Tech student trainee arising out of the contract of inplant training shall be resolved both by Maharashtra Institute of Technology and the industry with mutual cooperation. The decision of both Maharashtra Institute of Technology and the industry shall be final.</p>
		<p>Holding of Test and Grant of Certificate:</p> <p>The progress in inplant training of every student shall be assessed by the industry and Maharashtra Institute of Technology faculty from time to time. Every B.Tech student undergoing an inplant training shall be issued a certificate of Proficiency on completion of his training to the satisfaction of the industry.</p>
		<p>Offer of Stipend / Other Welfare Activities and Employment:</p> <p>It shall not be obligatory on the part of the Employer / Industry to offer any stipend and other welfare amenities available, if any, to the students of B.Tech courses undergoing an inplant training. However, if the industry desirous to do so, at will be a privilege for the students and also for Maharashtra Institute of Technology in view of the bonding of better understanding and cooperation forever.</p>
	(e)	<p>PRACTICAL EXAMINATION</p> <p>The Practical examination will be conducted after successful completion of the inplant training for which guide will be internal examiner and external examiner will be appointed by the university. The date of practical examination will be same for the students of a branch and will be notified by the university. The assessment of the practical examination shall consist of</p> <ol style="list-style-type: none"> 1. Seminar Performance 2. An oral on the project work done. 3. Assessment of the term work / report.